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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

Please amend claims 30, 32-34, 40-45, and 50-52 as follows:

1-29. (canceled)

30. (currently amended) A method of encapsulating an integrated circuit comprising the steps of:

providing a semiconductor chip;

providing a laminate defining first and second major faces, said laminate including an electrically conductive layer, and an underlying substrate supporting said electrically conductive layer;

forming at least one void in said laminate so as to extend from one of said major faces through said electrically conductive layer ~~at least as far as~~ into said underlying substrate, ~~but not as far as said second major face~~; and

encapsulating said semiconductor chip and said laminate with an encapsulant such that said encapsulant extends into said void to contact said underlying substrate.

31. (canceled)

32. (currently amended) A method of forming a laminate to lock an ~~encapsulant~~ encapsulant comprising:

~~providing a first~~ forming at least one continuous laminate layer;

forming a second laminate layer over ~~the first~~ said continuous laminate layer, so as to define an underlying cavity;

forming a third laminate layer over the said second laminate layer, so as to define a void portion over the said underlying cavity;

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forming a fourth laminate layer over ~~the~~ said third laminate layer, so as to define a void portion over the said void portion of ~~the~~ said third laminate layer;

forming a conductive layer over ~~the~~ said fourth laminate layer, so as to define a void portion over the said void portion of the said fourth laminate layer; and

forming a solder resist layer over the said conductive layer, so as to define a void portion over the said void portion of ~~the~~ said conductive layer.

33. (currently amended) The method of claim 32, wherein ~~the~~ said underlying cavity, the said void portion of the said third laminate layer, ~~the~~ said void portion of the said fourth laminate layer, ~~the~~ said void portion of the said conductive layer and ~~the~~ said void portion of the said solder resist layer are formed to collectively form a void.

34. (currently amended) The method of claim 33 further comprising:
placing a die over at least a portion of the said solder resist layer; and
forming an encapsulant over ~~the~~ said solder resist layer, over the said die and in the said void.

35–39. (canceled)

40. (currently amended) A method of encapsulating an integrated circuit comprising:
providing a die;
providing a substrate having at least one continuous laminate layer and at least one resin layer over said continuous laminate layer;
forming at least one laminate layer over the said at least one resin layer;
forming a void in the said at least one resin layer and ~~the~~ said at least one laminate layer such that a portion of the said void located in the said at least one resin layer is below a remaining portion of the said at least one laminate layer, wherein said void does not extend through said continuous laminate layer;
placing the said die over the said at least one laminate layer; and

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encapsulating the said die by forming encapsulant over the said at least one laminate layer, over the said die and in the said void.

41. (currently amended) The method of claim 40, wherein ~~the~~ said at least one laminate layer is formed by forming a conductive layer over ~~the~~ said at least one resin layer and forming a solder resist layer over ~~the~~ said conductive layer.

42. (currently amended) The method of claim 40, wherein ~~the~~ said void is formed by forming an underlying cavity in ~~the~~ said at least one laminate layer.

43. (currently amended) The method of claim 40, wherein ~~the~~ said encapsulant is formed in substantially all of the said void.

44. (currently amended) The method of claim 40, wherein ~~the~~ said at least one resin layer is formed from bismaleimide triazine laminate.

45. (currently amended) The method of claim 40, wherein ~~the~~ said at least one resin layer is formed from FR-4 epoxy-glass laminate.

46-49. (canceled)

50. (currently amended) The method of claim 33, wherein ~~the~~ said void has a varying profile.

51. (currently amended) The method of claim 50, wherein ~~the~~ said void having a varying profile is formed by a process selected from the group consisting of drilling, stamping, chemical etching, and combinations thereof.

52. (currently amended) The method of claim 50, wherein ~~the~~ said void having a varying profile is formed having a T-shaped profile.

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Please add claim 53 as follows:

53. (new) The method of claim 33, wherein said void extends into said laminate, but not entirely through said continuous laminate layer.